



U.S. Patent Application Serial No. 09/960,399  
Attorney Docket No.: 011225

**IN THE TITLE:**

Please amend the title of the invention, in its entirety, so as to read as follows:

-- A SEMICONDUCTOR INTEGRATED CIRCUIT AND FABRICATION  
PROCESS HAVING COMPENSATED STRUCTURES TO REDUCE  
MANUFACTURING DEFECTS --.

**IN THE SPECIFICATION:**

Amend the specification as follows:

Page 1, paragraph starting at line 25, has been amended as indicated below:

a' In a flash memory, writing and erasing of information is done by injection and pulling out of hot-carriers to or from a floating-gate electrode through a tunneling insulation film. In this operation, a high voltage is required for producing hot-carriers. For this purpose, a boosting circuit is provided in a peripheral circuit that cooperates with a memory cell for boosting a power supply voltage. The transistor used in such a peripheral circuit is required to operate at high voltage.

**IN THE CLAIMS:**

Please amend claims 16 and 17 as indicated below:

a 2 Sub B 16. (Amended) A semiconductor integrated circuit, comprising:  
a semiconductor substrate;

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